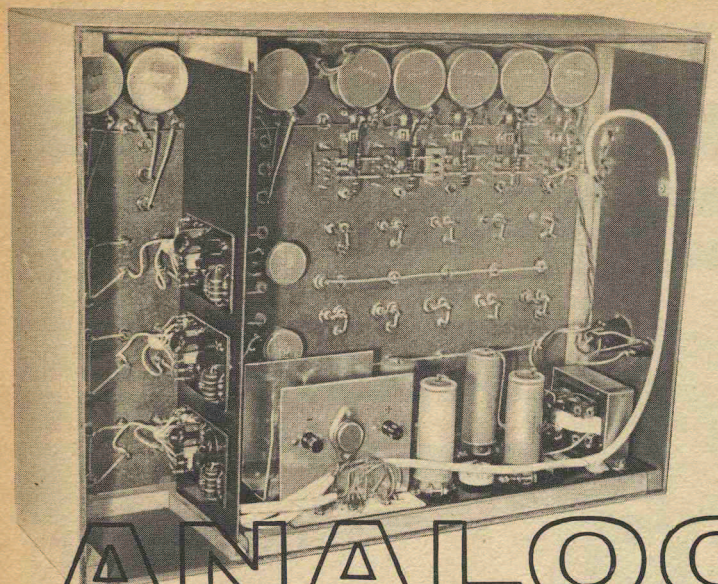


PEAC

By D. BOLLEN

ANALOGUE COMPUTER

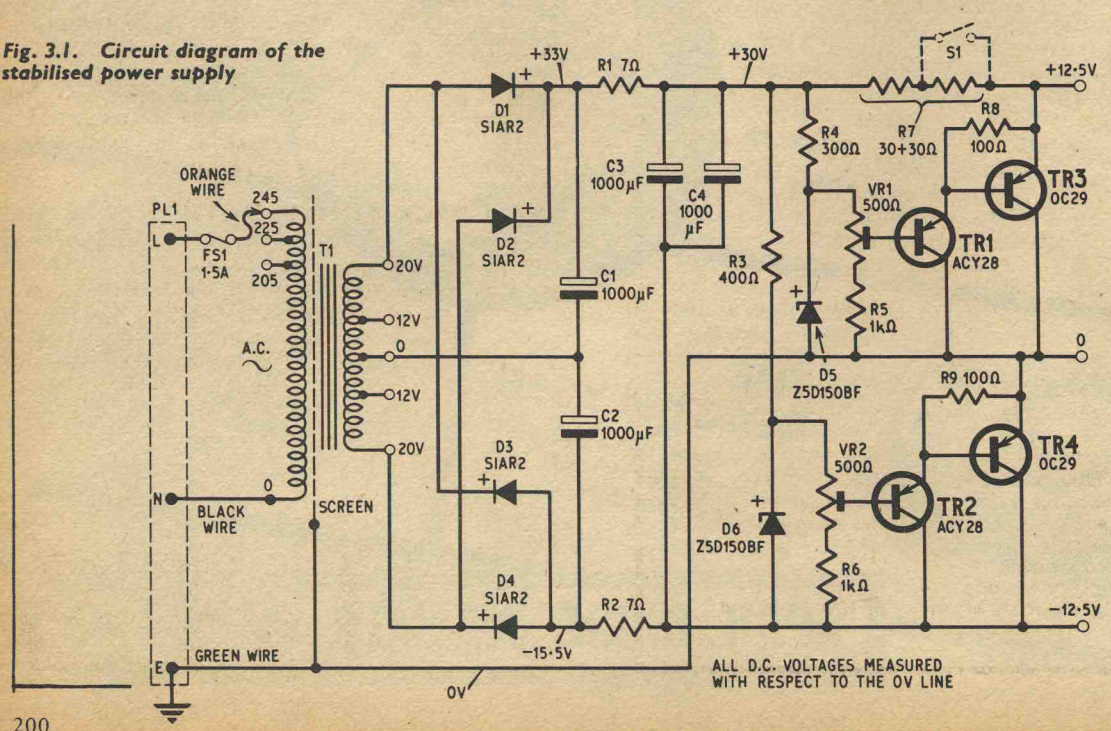
THE main design target for the PEAC power supply was a maximum voltage variation of not more than 1 per cent under all normal operating conditions. Several circuit configurations were tried, based upon either series or shunt regulation, but it was found that shunt regulation invariably gave the best performance for a given cost, plus the bonus of complete short-circuit protection. It was not considered to be a disadvantage for computer work, where nearly everything is switched on for most of the time, that a shunt regulated supply would be wasteful of power under no-load conditions.

The current reserve of the stabilised supply will just be sufficient to cater for the needs of UNITS "A to D". If further expansion of the computer is contemplated, beyond the inclusion of UNIT "D", a subsidiary unstabilised supply can be added to the computer at a late stage of construction, to power the relays of UNITS "B" and "D", and thus make available some extra current from the stabilised supply.

STABILISED POWER PACK

The circuit of Fig. 3.1 is based on a small, standard type of rectifier transformer, with bridge rectification

Fig. 3.1. Circuit diagram of the stabilised power supply



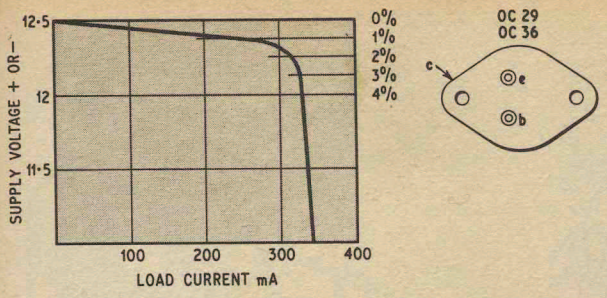


Fig. 3.2. Performance curve of stabilised power supply

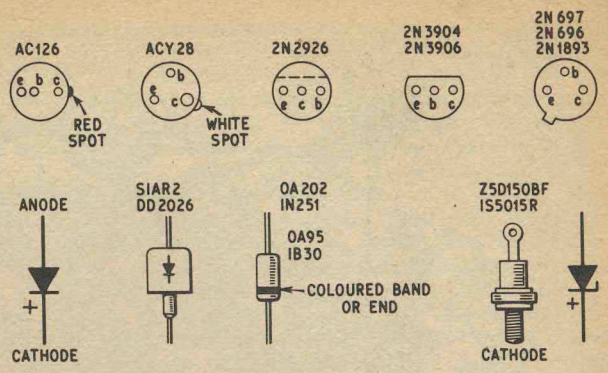


Fig. 3.3. Transistor and diode key

followed by two shunt regulators arranged in series to give positive and negative outputs relative to a zero voltage earthed centre-tap. Diodes D1–D4 provide full-wave rectification of the 40V r.m.s. nominal transformer output. Capacitors C1 and C2 are wired in series, with their common connection taken to the transformer centre-tap, and this doubles the capacitor voltage rating without the need for bleeder resistors. R1 and R2 achieve some measure of preliminary ripple smoothing while dropping the unregulated d.c. voltage to a safe value for C3 and C4.

COMPONENTS . . .

UNIT "A" POWER PACK

Resistors

R1, R2 7Ω 0·7A power resistors 5% (2 off)
R3 400Ω 5W wirewound 5%
R4 300Ω 5W wirewound 5%
R5, R6 1kΩ 2W carbon 10% (2 off)
R7 60Ω 0·7A power resistor 5% (two 30Ω in series, see text)
R8, R9 100Ω 1W carbon 10% (2 off)

Potentiometers

VR1, VR2 500Ω 3W panel mounting, wirewound (2 off)

Capacitors

C1–C4 1,000μF elect. 50V d.c. 900mA rippled (4 off)

Transformer

T1 Rectifier transformer. Standard mains primary. Secondary, 20V–0–20V 0·7A (Radiospares)

Diodes

D1–D4 S1AR2 (Westinghouse) *or* DD2026 (Lucas) (4 off)
D5, D6 Z5D150BF (STC) *or* IS5015R (Texas) (see text) (2 off)

Transistors

TR1, TR2 ACY28 (STC) *or* AC126 (Mullard) (2 off)
TR3, TR4 OC29 *or* OC36 (Mullard) (2 off)

Miscellaneous

Four capacitor clips to fit C1–C4
S.R.B.P. panel 4in × 12in × $\frac{1}{16}$in or $\frac{1}{8}$in
4 B.A. and 6 B.A. assorted screws, nuts, washers, and solder tags
Insulated sleeving
20 s.w.g. tinned copper wire
16 s.w.g. sheet aluminium 2 off 4in × 4in, and 2 off $1\frac{1}{2}$in × $1\frac{3}{4}$in

SHUNT REGULATORS

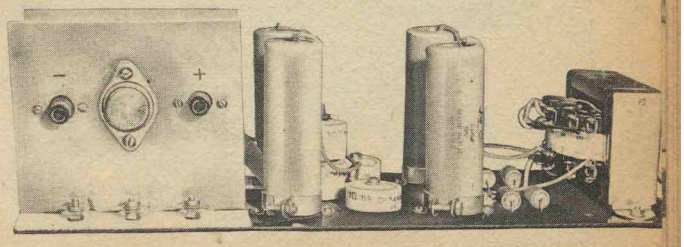
To understand the action of the twin shunt regulators, temporarily assume that the −12·5V output terminal is at zero voltage. The centre-tap and the positive outputs will then be positive in relation to the negative output. TR3 and TR4 collector-emitter voltages are both clamped at 12·5V, and the unregulated d.c. voltage is dropped across R7. Therefore, the voltage appearing at the junction of R7 and TR3 emitter is +25V relative to the assumed zero rail, with the centre-tap output at +12·5V. As all three output terminals are floating, it is a simple matter to connect the centre-tap output to an external earth and classify it as the zero voltage rail, with the other terminals forming positive and negative regulated outputs.

VR1 setting will determine the voltage across TR3, and VR2 the voltage across TR4. The range of adjustment of VR1 and VR2 is sufficient to allow for regulator diode (D5 and D6) tolerances on nominal voltage of ±15 per cent, and will therefore permit the use of manufacturers' rejects or "bargain" price regulator diodes. 10W diodes are specified for D5 and D6 in the Fig. 3.1 circuit, to achieve a low dynamic resistance, and reduce the short-term thermal changes which are inevitable when smaller regulator diodes are run at high temperatures.

Fig. 3.2 will give an idea of the capabilities of the regulated power supply, and maximum current limits. If an optional press-button switch is wired across one half of R7 (Fig. 3.1) output current can almost be doubled for short periods, and special purposes. The prolonged use of this extra current facility will, however, result in mains transformer overheating.

POWER PACK CONSTRUCTION

Low cost semiconductors were used throughout the prototype power pack. The diodes D1–D4 should have a p.i.v. rating of not less than 100V, and a maximum current rating of 1A or more. It is advisable to check all diodes with an ohmmeter, for high reverse resistance and correct polarity. The D5 and D6



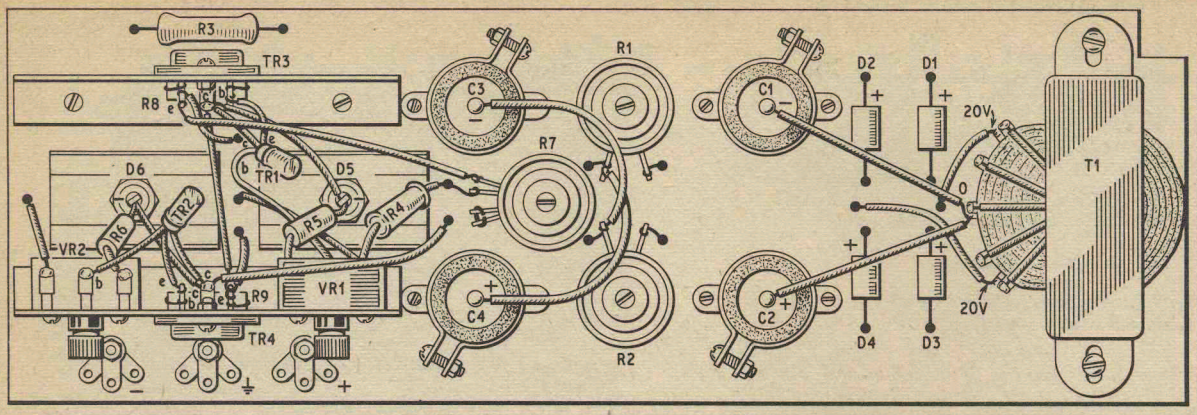


Fig. 3.4 Power supply component layout

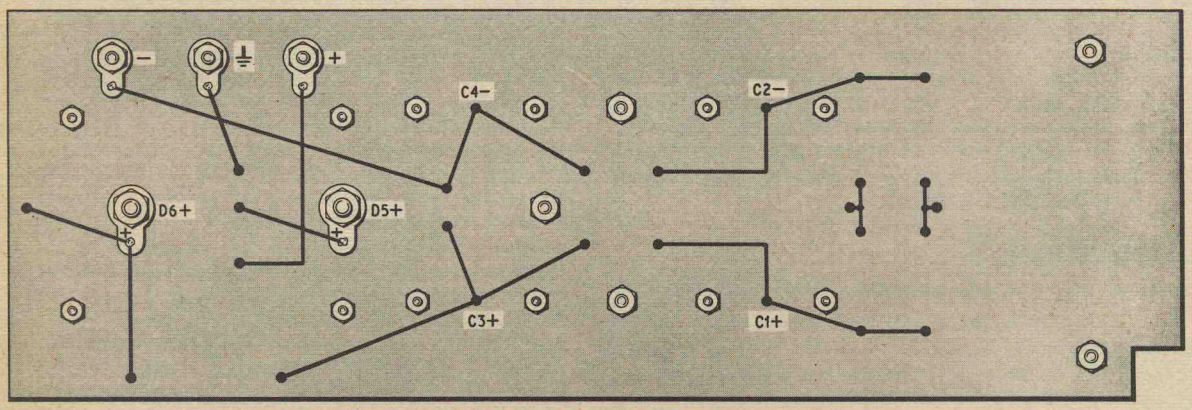


Fig. 3.5 Underside wiring of power supply panel

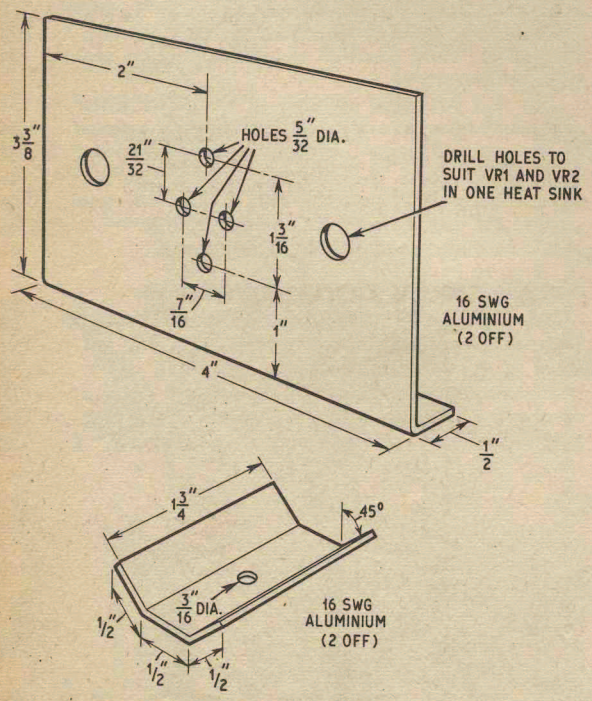


Fig. 3.6. Power supply heat sink details

measured voltage, when passing a current of about 100mA, can fall anywhere within the limits 12·5–17·5V.

If a choice exists, TR1–TR4 can be selected for highest *beta* gain, but matching is not necessary. Collector-emitter leakage currents of TR1 and TR2, with open circuit base, will preferably be below about 200μA at normal room temperature.

It is seriously recommended that the reader who intends to build PEAC should adhere closely to the semiconductor types specified here, and not consult other lists of equivalents. A key to transistor and diode connections appears in Fig. 3.3, and this covers all the semiconductors used in PEAC circuits.

Power pack components are assembled on a $\frac{1}{16}$in or $\frac{1}{8}$in s.r.b.p. panel measuring 4in × 12in. The panel sits on the wooden framework at the bottom of the UNIT "A" box. Component layout appears in Fig. 3.4, with the underside wiring in Fig. 3.5. Heat sinks for TR3, TR4, D5, and D6 are made up from 16 s.w.g. aluminium sheet, and measurements are given in Fig. 3.6.

First drill the s.r.b.p. chassis panel to accept hardware and wires, using Fig. 3.5 as a guide. Mount the mains transformer, capacitor clips, power resistors, and the three output terminal screws. Attach the regulator diodes, with their heat sinks and solder tags, to the panel, taking care not to damage the diode top terminals. Bolt TR4, VR1, and VR2 to the appropriate heat sink, solder R9 to TR4 emitter and base pins, and install the assembly on the s.r.b.p. panel. Similarly, bolt TR3 to its heat sink, complete with R8, and fix to panel.

Both power transistors should have a solder tag attached to their upper mounting bolts to make convenient connection to transistor collectors. Without insulating washers, TR3 and TR4 heat sinks will be "live", but damage is unlikely to result in the event of an accidental short-circuit.

Insert capacitors C1–C4 in clips, with polarity as indicated on Fig. 3.4. Also observe correct polarity when mounting diodes D1–D4. Before wiring up all components, insert R3 in the panel, alongside TR3 heat-sink.

COLOUR CODED WIRE

Wiring can start at the input end of the panel, with 6in lengths of orange, black, and green multi-stranded wire soldered to the live, neutral, and screen tags on the mains transformer. Red and blue wires are reserved exclusively for 12·5V d.c. positive and negative supply rails, with green wiring as the common earth throughout the computer.

Wire colour coding is almost essential for computer circuit interconnection, as it enormously simplifies fault tracing and assembly. However, the wiring of individual circuits, such as the power pack panel, can take the form of single colour sleeved 20 s.w.g. tinned copper wire.

It will be noticed (Fig. 3.4) that TR1 and TR2 are supported only by their leads, and this is to allow best positioning for good ventilation, well away from heat sinks. In the prototype R7 was made up from two 0·7A power resistor sections, to allow for the optional extra current facility mentioned earlier.

When power pack wiring is completed and checked, multiple solder tags can be fitted to the three output terminal screws.

TESTING THE POWER PACK

Connect the transformer input leads to the mains socket on the side panel of the UNIT "A" box, with the organge lead taken via FS1 (see Fig. 2.10 and Fig. 3.1), and, also join the neon indicator leads to the live and neutral mains socket screws.

Turn VR1 and VR2 fully anticlockwise and switch on. A quick check with a voltmeter will show if there is any serious departure from the voltages shown in Fig. 3.1. If any overheating of heat sinks or mains transformer seems imminent, switch off immediately and locate fault.

To set up the power pack, apply voltmeter leads to earth and positive output terminal, and advance VR1 for a reading of 12·5V. Repeat the procedure for the negative output and VR2. If it is impossible to bring an output to 12·5V, this will indicate a wiring fault or trouble with a regulator diode.

After the power pack has been left on for some time, VR1 and VR2 can be finally trimmed for exact outputs of $\pm$12·5V. With no external load on the power supply, TR3 and TR4 heat sinks can be expected to run fairly warm.

To ensure that power pack regulation conforms to the curve of Fig. 3.2, positive and negative outputs can be loaded by a selection of 5W resistors in series with an ammeter, while voltage is still being monitored. A worst case variation of 2 per cent change in voltage for 300mA change in current should be taken as an acceptable performance limit. When one half of R7 is temporarily shorted out, at least 50 per cent more current should be available before voltage drops beyond 2 per cent.

Locate the power pack inside the UNIT "A" box, and wire outputs to the main terminals TL1, TL2, and TL3. Voltage source dial alignment and setting up details will be discussed later, but a few rough checks with power on are in order, to see that all voltage source sockets and switches are functioning correctly.

OPERATIONAL AMPLIFIER

The most important analogue computing circuit is the operational amplifier; so named because it will perform a number of mathematical operations, such as addition, subtraction, change of sign, multiplication by a constant, division by a constant, and integration. All the thinking behind "op-amp" design is concerned with making the circuit as unobtrusive as possible, so that it can be regarded purely as an operational "black box".

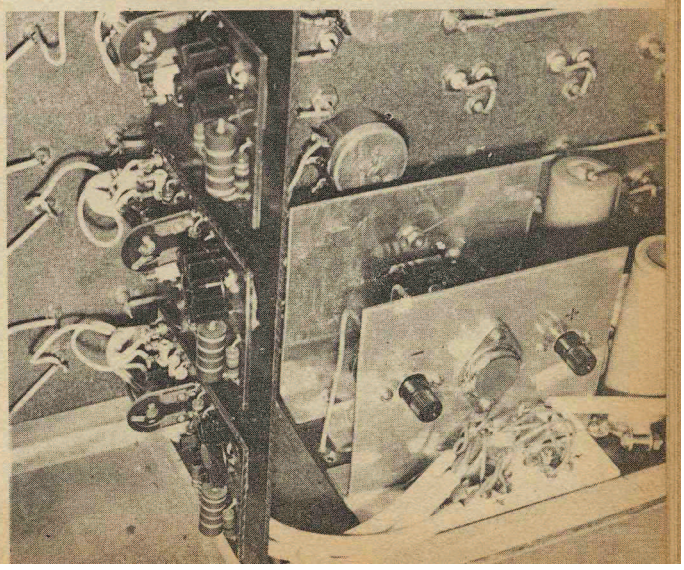
An analogue computer d.c. operational amplifier should comply with the following general requirements.

(a) Direct coupling between all stages to handle d.c. signals. Input and output terminals at earth potential in the absence of a signal, with 180 degree phase change (inversion) between input and output. Output voltage swings both positive and negative in relation to earth, and as large as the computer reference voltage ($\pm$10V).
(b) Large voltage gain in the open-loop configuration.
(c) Low output impedance.
(d) High input impedance.
(e) Very low input current.
(f) Sufficient bandwidth to cause negligible phase shift or attenuation of a signal up to the highest frequencies encountered.
(g) Insignificant output voltage drift over several hours.
(h) Good margin of stability when subjected to a wide range of different input, output, and feedback conditions.

Performance figures for UNIT "A" operational amplifiers are given in the Table 3.1, but to fully understand how some of the design problems are solved it is necessary to consult the actual "op-amp" circuit of Fig. 3.7.

OPERATIONAL AMPLIFIER CIRCUIT

The input stage of circuit Fig. 3.7 consists of a long-tailed pair (TR1, TR2), offering the advantages of high voltage gain, near zero input offset voltage relative to



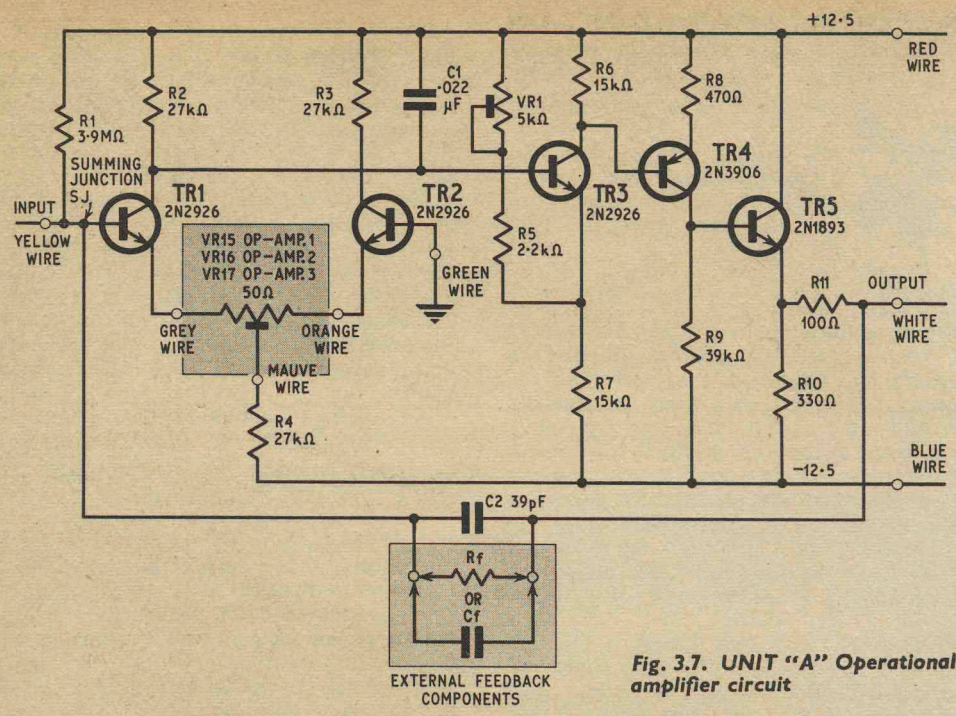


Fig. 3.7. UNIT "A" Operational amplifier circuit

COMPONENTS . . .

UNIT "A" OPERATIONAL AMPLIFIER

The following items are for a single amplifier, and are required in triplicate to cover the three amplifiers employed in UNIT "A".

Resistors

R1 3·9MΩ 5% carbon film
R2–R4 27kΩ 5% carbon film (3 off)
R5 2·2kΩ
R6, R7 15kΩ (2 off)
R8 470Ω
R9 39kΩ
R10 330Ω 2W
R11 100Ω
All ±10%, ½W carbon composition, except where otherwise stated

Potentiometer

VR1 5kΩ vertical skeleton pre-set

Capacitors

C1 0·022μF miniature polyester 250V d.c.
C2 39pF polystyrene 125V d.c.

Transistors

TR1–TR3 2N2926 orange (General Electric) *or* 2N3904 (Motorola) (3 off)
TR4 2N3906 (Motorola)
TR5 2N1893 (Bentron), 2N696, *or* 2N697 (General Electric).

Miscellaneous

S.r.b.p. panel 2in × 2¾in
Eight small turret tags
TO-5 transistor cooler Type BC105B (Bentron)
6 B.A. screws, nuts, and spacers
Stranded core p.v.c. wires; red, green, blue, orange, mauve, grey, yellow, and white
12in × 4in s.r.b.p. amplifier mount

Note: All transistors and cooler can be obtained from Rastra Electronics Ltd., 275–281 King Street, Hammersmith, W.6.

earth, and low drift with change in temperature when TR1 and TR2 are closely matched. The long-tailed pair also gives good rejection of drift induced by changes in supply voltage, and has a reasonably large input impedance at low collector current levels.

An input signal will undergo a phase change of 180 degrees between the base and collector of TR1, and the voltage datum level is shifted away from earth towards the positive rail voltage. Ignoring for the moment C1, the signal is passed straight to the base of TR3.

VR1, R5, and R7 form an adjustable potential divider across positive and negative supply rails, and the VR1 setting determines the working points of direct coupled stages TR3, TR4, and TR5. Front panel control VR15 sets the amplifier input at zero volts, while VR1 does the same for the output.

TR3, while contributing some voltage gain, also introduces another 180 degree change of phase, to bring the overall phase difference between the amplifier input and TR3 collector to zero. Obviously, the voltage at the collector of TR3 will be even closer to positive rail voltage than the collector of TR1, but this cumulative voltage shifting can be virtually eliminated by using a *pnp* transistor for TR4. At the same time, TR4 common emitter stage brings more voltage gain and another and final phase change of 180 degrees.

So, the situation at the collector of TR4, when VR15 and VR1 are at correct settings, will be no overall voltage shift, a total phase difference of 180 degrees, and a total voltage gain in the region of 5,000.

Finally, the addition of an emitter follower stage provides the low input impedance required for driving a variety of useful loads, without unwanted circuit complications. TR5 causes negligible further voltage shifting, adds no change of phase, and with a voltage gain very close to unity, will simply reduce the output impedance of the operational amplifier without modifying its other characteristics.

IMPORTANCE OF HIGH OPEN-LOOP GAIN

The ideal operational amplifier would have an infinite voltage gain when no feedback resistor was present, but since this is unattainable in practice, the effect of a finite open-loop gain on amplifier accuracy must be examined.

In Fig. 3.8, selected values of open-loop gain $-A$ are plotted against closed-loop gains $-G$, and percentage amplifier error. Closed-loop gains are normally restricted to 0·1–50 as this caters for almost all operational conditions, and it is seldom required to extend these limits. A different set of circumstances apply when the op-amp is used for integration, and these will be considered in detail later.

Very high $-A$ gains bring attendant drift and stability problems, and this in turn demands a larger number of components and more complicated circuitry to keep drift and stability within acceptable limits. At the opposite extreme, very simple amplifier circuits can

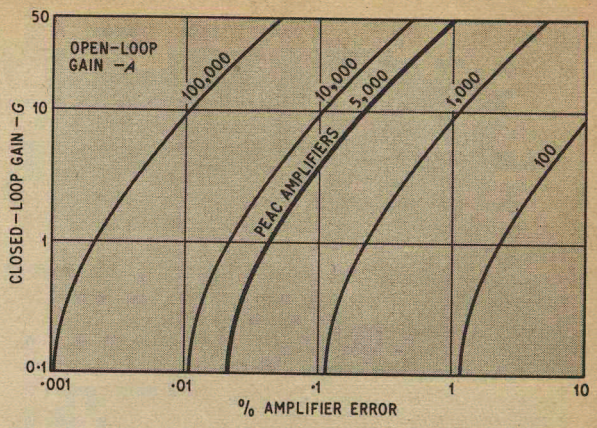


Fig. 3.8. Open-loop gain plotted against closed-loop gains and percentage amplifier error

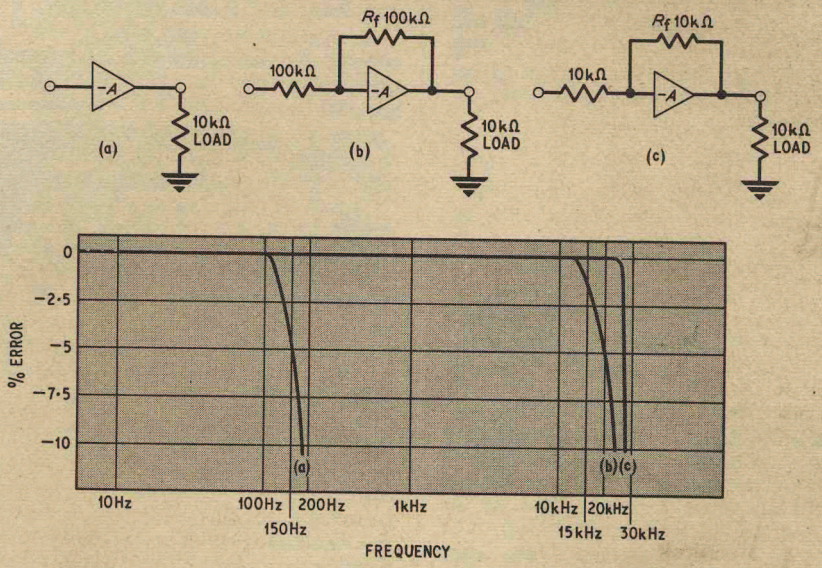


Fig. 3.9. Amplifier frequency response

TABLE 3.1

UNIT "A" OPERATIONAL AMPLIFIER. TYPICAL PERFORMANCE

Supply voltage ±12·5V ±0·5%
Open-loop voltage gain 5,000 d.c.—100Hz. 200 at 10kHz
Maximum output voltage ±10V for loads >2kΩ
±5V for loads >300Ω
Input impedance 40kΩ approx.
Input current 0·005μA for 1V out
Closed-loop frequency response 0–10kHz within 1% when R_f = 100kΩ
Equivalent input drift ±0·5mV per hour
Input offset voltage and current almost zero when amplifier correctly balanced
R.M.S. noise, referred to input with input open circuit 200μV
Normal maximum range of plug-in components
R_{in} 2–100kΩ
R_f 10–100kΩ
C_f 1–0·01μF
Stability unconditional with all normal problem layouts

be built to yield $-A$ gains in the region of 100–1,000, but when $-G$ approaches 50 the errors of such amplifiers would be near 10 per cent. Thus, if a low value for $-A$ was chosen, for the sake of simplicity, the range of available closed-loop gains would have to be restricted if the error was not to exceed one or two per cent, and this would place severe limitations on the operational flexibility of the amplifier.

It was assumed that PEAC operators would not wish to employ plug-in computing components with a selection tolerance better than, say, ±1 per cent. Therefore, the error contributed by the amplifier will preferably be less than external component errors, but not so small as to call for ridiculous extremes of circuit sophistication. The thickened curve of Fig. 3.8, corresponding to $-A = 5{,}000$, shows that the maximum error contribution of UNIT "A" amplifiers is 1 per cent or less for $-G$ gains of less than 50.

BANDWIDTH AND STABILITY

A direct coupled amplifier of the Fig. 3.7 type will display an almost constant phase change of exactly 180 degrees over a range of frequencies from d.c. to

about 20kHz. Thereafter, with increasing frequency, the phase angle will begin to shift until, at several hundred kHz, and especially when the amplifier has a high gain, sufficient positive feedback is present to cause sustained oscillation. To counteract this instability, small capacitors are suitably situated in the op-amp circuit to reduce gain at critical frequencies, and it follows that the use of such capacitors will place a limitation on the available frequency response of the amplifier.

C1 of Fig. 3.7 will block the unwanted high frequency content of incoming signals, and plays a major role in determining the bandwidth of the amplifier. If C1 is reduced in value, bandwidth will be increased, but so will the likelihood of instability. Needless to say, any form of instability will be highly detrimental to accuracy, and must be avoided at all costs. C2 works in a different way, by introducing negative feedback and consequent loss of gain at very high frequencies. Both capacitors act together to combat instability under the very varied conditions of operational amplifier use.

The measured frequency response of a representative UNIT "A" amplifier is given in Fig. 3.9, and is very linear up to the well-defined break frequencies of (a) open-loop, (b) with feedback resistor of 100 kilohm, and (c) when R_f = 10 kilohm.

DRIFT

If a d.c. amplifier is adjusted so that its output voltage is zero when there is no input signal, over an interval of minutes, hours, or days—depending on the amplifier, its power supply, and its surroundings—a spurious voltage will begin to appear at the output. A poor amplifier in adverse conditions will require frequent manual adjustments to keep its output at zero. Fortunately, drift errors are very small when an operational amplifier is used for summing and sign changing, due to the presence of a feedback resistor, and no adjustment of the amplifier will be called for during intervals of perhaps several hours, except in applications requiring a very high degree of accuracy. However, when the operational amplifier is being used as an integrator, with a capacitor in its feedback loop, it is quite possible for drift errors to exceed 1 per cent within a space of less than an hour if suitable precautions are not taken.

The figure quoted in Table 3.1 for drift is the amount of input voltage, either positive or negative, required at the amplifier summing junction to reset the amplifier output to zero after it has been allowed to drift for one hour following a preliminary computer warm-up period. In practical terms, a drift of about ±0·5mV

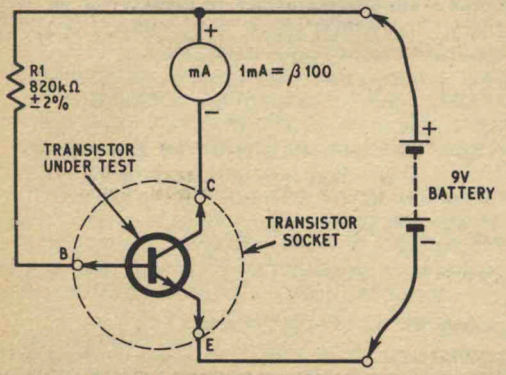
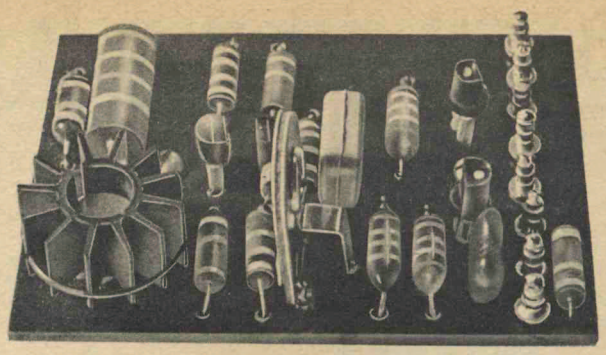


Fig. 3.10. Transistor test-rig. Note: reverse battery connections and milliammeter for pnp



per hour is not likely to prove to be too troublesome with most PEAC applications. Full scale analogue computers are sometimes installed in a temperature controlled computing room, and this considerably improves drift performance.

TRANSISTOR SELECTION

Several prototype UNIT "A" amplifiers were constructed using non-selected transistors, and about one third of the amplifiers failed to meet the specification of Table 3.1. Defects were due entirely to "spreads" in semiconductor characteristics, and disappointment will be avoided if all amplifier semiconductors are tested before use.

It has already been mentioned that the long-tailed pair input stage transistors (TR1 and TR2 in Fig. 3.7) should be matched. In all nine transistors of the same type will be required for TR1, TR2, and TR3 in the three operational amplifiers, and it will assist the matching and selection process if, say, one dozen transistors are purchased at the same time. No wastage will be involved as "spare" transistors can later be used up in other PEAC circuits.

A simple test-rig circuit is given in Fig. 3.10 to facilitate the matching of TR1 and TR2, and the circuit can also be quickly adapted for checking other transistors. The test-rig could take the form of a transistor socket and resistor mounted on an odd piece of s.r.b.p., or Veroboard, with a testmeter employed as a milliameter.

Select each TR1–TR2 pair for near identical *betas* of 100 or more; this will dispose of six transistors. Do not attempt to pair off transistors of different types even if they do have the same *beta*. From the remaining transistors, choose three with the highest *beta* for TR3.

Although TR4 is a *pnp* transistor, it must be of silicon construction for low leakage drift. The majority of *pnp* silicon types at present on the market are unsatisfactory for use in the op-amp circuit because they exhibit almost no gain at all at very low collector current levels. Of all the types so far tested only the 2N3906 was found to be consistently good at low currents, therefore a suitable equivalent cannot be quoted. To check TR4, reverse the battery leads to the Fig. 3.10 test-rig, and switch connections to the milliameter before plugging in the *pnp* transistor. TR4 should display a *beta* of about 50 or more.

When handling plastic encapsulated transistors, which tend to look alike, take note that lead connections do not necessarily conform to a common pattern. In particular, notice the lead differences between types 2N2926 and its equivalent 2N3904, and remember that the 2N3906 is *pnp*. To avoid mishaps, always refer to Fig. 3.3 before applying current to the transistor.